REMARKS

Claim Rejections - 35 USC §112

Claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The rejected claim term is:

"encapsulating all of the volume around the semiconductor devices"

It is respectfully submitted that this claim term is clear and definite under 35 U.S.C. §112 both on its face and based on the Specification page 6, lines 19-22, which states:

> "Referring now to FIG. 4, therein is shown a cross-sectional view of the structure of FIG. 3 following application and molding of an encapsulant 400 to encapsulate all of the volume around the chips 102 and up to the level of the top surfaces 402 of the heat spreaders 300."

The Examiner stated:

> "The claims recite the limitation of "encapsulating all of the volume around the semiconductor devices."...[T]he specification and drawings of the application indicate that only the areas around the devices unoccupied by the substrate, the underfill, the heat spreader, and the thermal interface material are filled by the encapsulant. It is unclear whether the Applicant is trying to claim that all of the volume immediately surrounding the semiconductor device (except that filled by other claimed components) is filled with the encapsulant; whether the volume around the semiconductor device and between the heat spreader and substrate is filled by only the encapsulant, or whether the assembly itself consists only of the claimed substrate, underfill, heat spreader, semiconductor device, and thermal interface material, with the encapsulant filling all other space in the die package. For the purpose of examination, the examiner is interpreting the "all of the volume" limitation according to the first situation listed supra (i.e., the volume immediately surrounding the semiconductor device (except that filled by the other claimed components) is filled with encapsulant." [deletions and underlining for clarity]

Applicants respectfully disagree with the Examiner's alternative characterizations of the "encapsulating..." claim term because of the holding in All Dental Prodx, LLC v. Advantage Dental Products, Inc., 309 F.3d 774 (Fed Cir. 2002) where the CAFC held that,

where the claim term was properly described in the specification, it was definite and clear in the claim as a result.

The Examiner admits:

> "[T]he specification and drawings of the application indicate that only the areas around the devices unoccupied by the substrate, the underfill, the heat spreader, and the thermal interface material are filled by the encapsulant."

This is in keeping with the claimed limitation.

However, to advance prosecution of this application, the Applicants have elected to adopt the language suggested by the Examiner in order to remove any residual concerns regarding the meaning to the phrase "all of the volume". Support for the amendments to the claims is found in the specification and drawings as noted by the Examiner, is found in the Examiner's suggested language (including the language at the bottom of page 3 of the Office Action), and is found on page 6, lines 19-22 (because the void that is otherwise filled with the encapsulant may also include "other electronic components...assembled onto the substrate").

Entry of these amendments is proper in accordance with MPEP §714.13 because it is an amendment adopting an Examiner suggestion (to enumerate the items excluded from "all of the volume"), and because the amendment removes issues for appeal without raising new issues.

Claim Rejections - 35 USC §102

Claims 1-20 are rejected under 35 U.S.C. §102(e) as being anticipated by Kirloskar et al. (U.S. Patent No. 6,933,176, hereinafter "Kirloskar").

Kirloskar provides a ball grid array integrated circuit package and process in which a semiconductor die is mounted to a surface of a substrate. Collapsible spacers are mounted to a heat spreader, the semiconductor die, and the substrate. The heat spreader is fixed such that the collapsible spacers are disposed between it and the semiconductor die and the substrate. A ball grid array is formed on a second surface of the substrate. The integrated circuit package is then singulated.

Regarding claims 1, 6, 11, 15, 16, and 20, the Applicants respectfully traverse the rejection of these claims since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Kirloskar of:

> "encapsulating all of the volume immediately surrounding the semiconductor devices except that volume filed by the substrate, the underfill between the semiconductor devices and the substrate, the thermal interface material applied to the semiconductor devices, the flat panel heat spreader attached to each semiconductor device, and other electronic devices assembled on the substrate, with open encapsulation"

The Examiner states in the Office Action dated September 2, 2005:

> "encapsulating the semiconductor devices...(column 4, line 60 – column 5, line 3) with open encapsulation...Note that Kirloskar discloses that all of the volume immediately surrounding the semiconductor device except that occupied by the substrate, the underfill, the heat spreader assembly, and the thermal interface material is occupied by the encapsulant (see figures 3I, 5I)." [deletions for clarity]

However, Kirloskar does not disclose that all of that volume is filled with encapsulant, because Kirloskar does not fill the substantial volume of the collapsible spacers with encapsulant. Thus, Kirloskar does not disclose encapsulating all of the claimed volume with encapsulation, but at column 4, line 67 – column 5, line 2, states:

> "The molding compound 128 encapsulates the semiconductor die 124, and the collapsible spacers 136 between the heat spreader 132 and the substrate 122" [underlining for clarity]

Thus Kirloskar makes clear that a significant portion of the encapsulated volume is filled by the collapsible spacers rather than the encapsulant. Thus, Kirloskar does not disclose encapsulating all of the claimed volume around the semiconductor devices with open encapsulation as now claimed in all the claims.

The Examiner also stated, in the Response to Arguments:

> "Since the collapsible spacers in Kirloskar could either be considered to be part of the heat spreader (figure 5F shows the spacers 136 and spreader 132 as one integral body) or part of the thermal interface material (spacers are formed of a thermally conductive material, and thus conduct heat from the substrate to the heat spreader), it appears to the Examiner that Kirloskar reads

> on the claim language taken in light of the Applicant's specification and disclosure (as explained in the 35 U.S.C. 112 rejections, supra).

However, this is not what Kirloskar discloses. Kirloskar specifically discloses that the spacers and the heat spreader are separate elements mounted to one another, not "one integral body", as clearly shown in FIG. 5F and as described at column 5, lines 24–26:

> "In FIG. 5F, however, the collapsible spacers 135 are mounted to the heat spreader 132" [underlining for clarity]

Thus, Kirloskar's spacers and heat spreader are separate elements mounted to one another, not "one integral body".

Additionally, concerning the Examiner's alternative suggestion that the spacers are "part of the thermal interface material", such is clearly not the meaning understood by persons of ordinary skill in the art for "thermal interface material". For example, the Wikipedia Encyclopedia at http://en.wikipedia.org/wiki/Thermal_interface_material, defines thermal interface material as:

> "A Thermal Interface Material (aka TIM) is used to fill the gaps between thermal transfer surfaces, such as between microprocessors and heatsinks, in order to increase thermal transfer efficiency. These gaps are normally filled with air which is a very poor conductor.
>
> They take many forms. The most common is the white-colored paste or thermal grease, typically silicone oil filled with aluminum oxide, zinc oxide, or boron nitride.
>
> Another type of TIM are the phase-change materials. These are solid at room temperature but liquefy and behave like grease at operating temperatures." [underlining for clarity]

Kirloskar's collapsible spacers do not meet this well-understood meaning of a thermal interface material.

Additionally, in reciting the specific excluded elements as suggested by the Examiner, the claims now specifically refer to the previously claimed thermal interface material which is now explicitly included in the claimed excluded volume:

> "the thermal interface material applied to the semiconductor devices"

Kirloskar's collapsible spacers are not thermal interface material applied to the semiconductor devices.

It is therefore respectfully submitted that independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending directly or indirectly therefrom, are not anticipated by Kirloskar under 35 USC §102(e) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Withdrawal of the rejection is therefore respectfully requested.

Regarding claims 2, 7, 12, and 17, these dependent claims each depend respectively from independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 2, 7, 12, and 17 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

Regarding claims 3, 4, 8, 9, 13, 14, 18, and 19, these dependent claims directly or indirectly each depend respectively from independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 3, 4, 8, 9, 13, 14, 18, and 19 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra.*

Regarding claims 5 and 10, these dependent claims each indirectly depend respectively from independent claims 1 and 6, and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and

additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 5 and 10 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

It is therefore respectfully submitted that the independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are not anticipated by Kirloskar under 35 USC §102 and are not obvious in combination under 35 USC §103 with the other cited references.

Claim Rejections - 35 USC §103

Claims 1-4, 6-9, and 11-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Combs et al. (U.S. Patent No. 6,734,552, hereinafter "Combs") in view of Lin et al. (U.S. Patent No. 5,450,283, hereinafter "Lin").

Combs provides an enhanced thermal dissipation integrated circuit package having a semiconductor die on a substrate, a heat sink having an extending finger, a thermally conductive element thermally coupled with an interposer between both the semiconductor die and the heat sink, and an encapsulant material encapsulating the thermally conductive element and the heat sink. The thermally conductive element does not directly contact the semiconductor die.

Lin provides a thermally enhanced semiconductor device having an exposed backside, and a method for making the same. A PC board substrate has a pattern of conductive traces on both upper and lower surfaces of the substrate. A semiconductor die is flip-mounted to the upper surface of the substrate. Solder bumps electrically connect the die to the conductive traces. An underfill couples the active side of the die to the upper surface of the substrate. A package body is formed around the perimeter of the die leaving the inactive backside exposed for enhanced thermal dissipation. The inactive backside can also be coupled to a heat sink for increased thermal dissipation. A plurality of solder balls electrically connected to the conductive traces is attached to the lower surface of the substrate.

Regarding claims 1, 6, 11, 15, 16, and 20, the Applicants respectfully traverse the rejection on the grounds that the Applicants' claimed combination would be patentable over

Combs in view of Lin since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Combs or Lin taken as a whole of:

"applying an underfill between the semiconductor devices and the substrate"

The Examiner states in the Office Action:

> "Combs indicates that the semiconductor device may be a flip chip (see figure 3), but fails to specifically disclose applying an underfill between the devices and the substrate."

Thus, the Examiner has acknowledged that Combs does not teach this combination.

The Examiner then states in the Office Action:

> "Lin discloses that it is standard in the art to apply an underfill between a flip chip device and a substrate in order to reduce the thermal mismatch between the chip and substrate, thus reducing the risk of breakage of the solder joints. Lin further indicates that underfills are advantageous in providing additional protection for the die from contaminants (see column 3, line 60 – column 4, line 15).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method and device of Combs, such that an underfill is applied between the device and the substrate, as suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide an underfill, in order to reduce the thermal stress on the solder joints, minimize the thermal mismatch between the substrate and die, and provide environmental protection for the active surface of the die (see Lin, column 3, line 40 – column 4, line 15)."

However, Combs does not teach or disclose anything about thermal mismatch or thermal stress between the chip and the substrate. Combs is only concerned about stress on the other side of the die, between the die and the heat sink, as shown by Combs at column 5, line 60 – column 6, line 10:

> "However, to avoid imparting stress to the semiconductor die 130, the adaptor element 122 does not directly contact the semiconductor 130 surface...
>
> An adhesive layer 119, having both high thermal conductivity and deformability to minimize stress...may be used to join the adaptor element 122 to the heat sink 110...
>
> The adaptor assembly 120 may also include a polymeric thermal interface 124 between the semiconductor die 130 and the adaptor element 122...the coefficient of polymeric thermal expansion (CTE) of the thermal

> interface 124 is similar to that of silicon to minimize stress on the semiconductor die 130." [deletions for clarity]

The above shows that Combs' stress management teaches directly away from Lin by omitting the underfill which the Examiner states is "standard in the art", and instead teaches minimization of stress above the die between the die and the heat sink.

Combs' clear awareness of stress issues and Combs' clear omission of an underfill, as acknowledged by the Examiner, suggests that, contrary to the Examiner's suggestion, stresses were either absent beneath Combs' die or Combs did not consider such stresses to be important. Clearly, Combs did recognize and did address the issue of die stresses. But just as clearly, Combs disclosed nothing about stresses beneath the die, and in fact omitted stress management beneath the die while teaching stress management above the die. For this reason, it is clear that Combs regarded stress management beneath the die as unimportant, and therefore the motivation for incorporating any of the teachings of Lin into Combs would come from the teachings of the present invention and not from the cited prior art.

Thus, it is respectfully submitted that each reference has not been taken as a whole but only portions of each reference have been combined, using the claimed invention as an instruction manual, and this is impermissible because the CAFC has stated:

> "Here the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re* Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992)." [deletions for clarity]

Accordingly, neither Combs nor Lin, taken as a whole, provides a teaching, suggestion, or motivation for the combination of Combs in view of Lin, as suggested by the Examiner and as taught and claimed by the Applicants of:

"applying an underfill between the semiconductor devices and the substrate"

Accordingly, and based upon the above, it is respectfully submitted that claims 1, 6, 11, 15, 16, and 20 are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Therefore, allowance of claims 1, 6, 11, 15, 16, and 20, and the claims respectively depending therefrom, is respectfully requested.

Regarding claims 2, 7, 12, and 17, these dependent claims each depend respectively from independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 2, 7, 12, and 17 is therefore respectfully requested because of *In re* Fritch and *In re* Vaeck, *supra.*

Regarding claims 3, 4, 8, 9, 13, 14, 18, and 19, these dependent claims depend from respective independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 3, 4, 8, 9, 13, 14, 18, and 19 is therefore respectfully requested because of *In re* Fritch and *In re* Vaeck, *supra.*

It is therefore respectfully submitted that the independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are allowable under 35 U.S.C. §103(a) as being unobvious over Combs in view of Lin taken as a whole, to a person having ordinary skill in the art at the time the invention was made.

Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lee et al. (U.S. Patent Publication No. 2001/0019181, hereinafter "Lee") in view of Akram et al. (U.S. Patent No. 6,534,858, hereinafter "Akram").

Lee provides a heat slug-equipped package and fabrication method. The package includes a chip located on a substrate with a signal transferring device electrically connected between them. Solder balls electrically connect the substrate to external circuits. Molding compound protects the chip and signal transferring device. The heat slug is capped over the molding compound through a conductive glue. All area of the upper surface of the heat slug is exposed to the ambient to improve the capability of spreading heat.

Akram provides an assembly and methods for a packaged die on a printed circuit board with heat sink encapsulant. A heat sink is provided on an upper surface of a semiconductor chip by placing a heat-dissipating material thereon which forms a portion of a glob top. The apparatus comprises a semiconductor chip attached to and in electrical communication with a substrate. A barrier glob top material is applied to the edges of the semiconductor chip on the surface opposite the surface attached to the substrate to form a wall around a periphery of an opposing surface of the semiconductor chip wherein the barrier glob top material also extends to contact and adhere to the substrate. The wall around the periphery of the opposing surface of the semiconductor chip forms a recess. A heat-dissipating glob top material is disposed within the recess to contact the opposing surface for the semiconductor chip.

Regarding claims 1, 6, 11, 15, 16, and 20, the Applicants respectfully traverse the rejection on the grounds that the Applicants' claimed combination would be patentable over Lee in view of Akram since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Combs or Lin taken as a whole of:

> applying a thermal interface material to the semiconductor devices;
> encapsulating...the semiconductor devices...

The Examiner states in the Office Action:

> "...Lee discloses...applying a thermal interface material to the upper faces of the devices (see figures 2, 5d; paragraph 0025; noting that the thermal

> interface material is directly applied to the semiconductor device in the figure 2 embodiment, and in the figure 5d embodiment, the thin portion of the molding compound as well as the glue layer can be considered a thermal interface, as it enables heat transfer from the die to the heat spreader" [deletions for clarity]

However, with respect to the figure 2 embodiment, Lee does not teach or suggest applying a thermal interface material to the semiconductor devices, but in paragraph [0007], teaches that the space immediately above the semiconductor device is molding compound and air, not a thermal interface material:

> "FIG. 2 shows the package in the prior art 2...the substrate 20' and the heat spreader 32' is sealed with molding compound 30' but the top side of the heat spreader 32' exposed. Actually, there are many holes (not shown) through the heat spreader 32', and molding compound 30' is driven into the heat spreader 32 therethrough. Unfortunately, there may be defects on the molding compound 30' (e.g. some air may left in the molding compound), which would make the thermally conductive paths between the molding compound 30' and the heat spreader 32' discontinuous. The heat resistance between them is thus risen, and which makes the efficiency of heat spreading poor." [deletions and underlining for clarity]

Thus Lee does not teach applying a thermal interface material to the semiconductor devices in Fig. 2.

And in paragraph [0025] concerning the figure 5d embodiment, Lee teaches that the:

> "thermally conductive material is layered on the top surface of the molding compound. The heat-spreading device is capped atop the thermally conductive material and the molding compound, wherein the thermally conductive material acts as a material for thermal transfer from the molding compound to the heat-spreading device." [underlining for clarity]

Thus, in Fig. 5d, Lee applies the thermally conductive material to the molding compound, not to the semiconductor device. The Examiner then suggested that the molding compound is also a thermal interface as claimed by the Applicants. However, the Examiner's above reading of the claims is by the double inclusion of elements; i.e., reading two claimed elements on the one element in the reference. This renders the Examiner's reading indefinite and not anticipatory under *Ex parte* Kristensen, 10 USPQ2d 1701 (Bd. Pat. App. & Inter.

1989). (The Applicants' shunt and Applicants' seed layer cannot both be read on Ting's catalytic seed layer.)

The above shows that Lee does not teach or suggest each of the separate steps of applying the thermal interface material to the semiconductor devices *and* encapsulating the semiconductor devices, and could not provide this teaching for a combination with Akram.

Similarly, Akram's heat-dissipating glob top 428 is a single element and not the separately claimed elements of applying a thermal interface material to the semiconductor devices, *and* encapsulating the semiconductor devices. Akram makes this clear at column 5, lines 39–44:

> "As seen in FIGS. 4 and 5, a barrier glob top 424 is applied to surround a periphery of the semiconductor chip 402 which seals and protects the semiconductor chip 402 and forms a recess or cavity 426. A heat-dissipating glob top 428 is disposed within the recess 426 as shown in FIG. 4."

The above shows that Akram does not teach or suggest each of the separate steps of applying the thermal interface material to the semiconductor devices and encapsulating the semiconductor devices, and could not provide this teaching for a combination with Lee.

Accordingly, neither Lee nor Akram provides the separate steps of applying the thermal interface material to the semiconductor devices and encapsulating the semiconductor devices, and there is thus no teaching, suggestion, or motivation in these references taken as a whole for the combination of Lee in view of Akram, as suggested by the Examiner and as taught and claimed by the Applicants of:

> applying a thermal interface material to the semiconductor devices;
> encapsulating...the semiconductor devices...

Accordingly, and based upon the above, it is respectfully submitted that claims 1, 6, 11, 15, 16, and 20, and the claims respectively depending therefrom, are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be

found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Regarding claims 1, 6, 11, 15, 16, and 20, the Applicants also respectfully traverse the rejection on the grounds that the Applicants' claimed combination would be patentable over Lee in view of Akram since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Lee or Akram taken as a whole of:

"applying an underfill between the semiconductor devices and the substrate"

The Examiner states in the Office Action:

"Lee fails to disclose applying an underfill between the devices and the substrate, but rather only discloses an epoxy adhesive."

Thus, the Examiner has acknowledged that Lee does not teach this combination.

The Examiner then states in the Office Action:

"It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Lee, such that the wirebonded chip is replaced by a flip chip with an underfill, as suggested by Akram. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use flip chips in the structure of Lee, because Akram shows that substantially the same package architecture, including the same approaches to thermal management are applied for both flip chip and wirebonded chip-on-board devices (see Akram, columns 1-3). It would thus be a matter of routine skill in the art to apply the method and structure taught by Lee to devices attached by any of the chip-on-board methods taught by Akram, in order to achieve the improved heat dissipation of the Lee-type package (see Lee, paragraphs 0009, 0010, 0030). Furthermore, a person skilled in the art would generally find a flip chip and underfill arrangement preferable over a wirebonding arrangement, since the wirebonding process is generally slower, more expensive, and less reliable than a flip chip process, and since the underfill material is selected to provide greater thermal matching between the substrate and the chip, as is well-known in the art."

However, Lee was filed over a year after Akram's parent patent issued, and Lee specifically taught and disclosed a wirebonding arrangement (as acknowledged by the Examiner), not a known flip chip arrangement, thus teaching away from Akram's earlier-

issued flip chip and underfill teachings. This, and the continued commercial production and usage of wirebonding arrangements even to this day, clearly contradict the Examiner's suggestion that:

> "a person skilled in the art would generally find a flip chip and underfill arrangement preferable over a wirebonding arrangement"

The above shows that Lee in fact teaches away from Akram's prior teachings by using a wirebonding arrangement and not applying an underfill.

Thus, it is respectfully submitted that each reference has not been taken as a whole but only portions of each reference have been combined, using the claimed invention as an instruction manual, and this is impermissible because the CAFC has stated:

> "Here the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re* Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992)." [deletions for clarity]

Accordingly, neither Lee nor Akram, taken as a whole, provides a teaching, suggestion, or motivation for the combination of Lee in view of Akram, as suggested by the Examiner and as taught and claimed by the Applicants of:

> "applying an underfill between the semiconductor devices and the substrate"

Accordingly, and based upon the above, it is respectfully submitted that claims 1, 6, 11, 15, 16, and 20 are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Therefore, allowance of claims 1, 6, 11, 15, 16, and 20, and the claims respectively depending therefrom, is respectfully requested.

Regarding claims 2-4, 7-9, 12-14, and 17-19, these dependent claims depend from respective independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 2-4, 7-9, 12-14, and 17-19 is therefore respectfully requested because of *In re* Fritch and *In re* Vaeck, *supra.*

Regarding claims 5 and 10, these dependent claims depend from respective independent claims 1 and 6, and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they depend and additionally claim non-obvious combinations thereof. Withdrawal of the rejections of claims 5 and 10 is therefore respectfully requested because of *In re* Fritch and *In re* Vaeck, *supra.*

It is therefore respectfully submitted that the independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending therefrom, are allowable under 35 U.S.C. §103(a) as being unobvious over Lee in view of Akram taken as a whole, to a person having ordinary skill in the art at the time the invention was made.

Response to Arguments

The Examiner stated that Applicants' arguments with respect to claims 1-20 have been considered but are moot in view of the new grounds of rejection. The Examiner's Response has been addressed above with respect the rejection under 35 USC §102 over Kirloskar, showing that Kirloskar's spacers and heat spreader are separate elements mounted to one another, not "one integral body", and that Kirloskar's collapsible spacers do not meet the well-understood meaning in the art of a thermal interface material.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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